1. (Amended) An assembly method for a semiconductor assembly, comprising:

providing a first substrate having a facing surface and having at least one lead having a portion thereof located on said facing surface of said first substrate, said at least one lead having at least one conductive pad disposed on the portion thereof located on said facing surface of said first substrate, said at least one conductive pad of said at least one lead of said first substrate having a thickness and having a contact surface area;

providing a second substrate having a facing surface and having at least one lead having a portion thereof located on said facing surface of said second substrate, said at least one lead having at least one conductive pad disposed on the portion thereof located on said facing surface of said second substrate, said at least one conductive pad of said at least one lead of said second substrate having a thickness and having a contact surface area;

providing a passivation layer on said facing surface of said first substrate, said passivation layer having a thickness greater than said thickness of said at least one conductive pad of said at least one lead of said first substrate such that said at least one conductive pad of said at least one lead of said first substrate is recessed a distance within an opening of said passivation layer;

forming an opening in said passivation layer at the location of said at least one conductive pad of said at least one lead of said first substrate;

attaching said first substrate to said second substrate, said at least one conductive pad of said at least one lead of said second substrate extending a distance within an opening of said passivation layer of said first substrate;

abutting said contact surface area of said at least one conductive pad of said at least one lead of said first substrate against said contact surface area of said at least one conductive pad of said at least one lead of said second substrate;

forming direct sliding movable contact between said contact surface area of said at least one conductive pad of said at least one lead of said first substrate and said contact surface area of said at least one conductive pad of said at least one lead of said second substrate, and establishing electrical communication therebetween; and

encapsulating said first substrate and said second substrate with an encapsulation material.

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2. The method of claim 1, wherein the step of attaching said first substrate to said second substrate further comprises the steps of:

forming a passivation layer by said providing a passivation layer on said facing surface of said first substrate; and

attaching said passivation layer to said facing surface of said second substrate with a layer of adhesive.

3. The method of claim 1, wherein the step of attaching said first substrate to said second substrate further comprises:

forming a passivation layer by said providing a passivation layer on said facing surface of said second substrate; and

attaching said passivation layer to said facing surface of said first substrate with a layer of adhesive.

4. The method of claim 1, wherein the step of attaching said first substrate to said second substrate further comprises:

covering one of said first substrate and said second substrate with a glob top which adheres to the facing surface of one of said first substrate and said second substrate.

Claim 5 is cancelled.

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56. The method of claim 1, wherein at least one of said facing surface of said first substrate and said facing surface of said second substrate includes at least one groove thereon.

57. The method of claim 1, wherein at least one of said first substrate and said second substrate comprises a flip chip.

58. The method of claim 1, wherein at least one of said first substrate and said second substrate comprises a silicon wafer.

59. (Amended) An assembly method for a semiconductor assembly, comprising:

providing a first substrate having a first surface and having at least one lead having a portion thereof located on said first surface of said first substrate, said at least one lead having at least one conductive pad disposed on said portion thereof located on said first surface of said first substrate, said at least one conductive pad of said at least one lead of said first substrate having a substantially flat surface area and having a thickness;

providing a second silicon substrate having a first surface and having at least one lead having a portion thereof located on said first surface of said second substrate, said at least one lead having at least one conductive pad disposed on said portion thereof located on said first surface of said second substrate, said at least one conductive pad of said at least one lead of said second substrate having a substantially flat surface area and having a thickness;

providing a passivation layer on said first surface of said first substrate, said passivation layer having a thickness greater than said thickness of the at least one conductive pad of said at

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least one lead of said first substrate, said at least one conductive pad of said at least one lead of said first substrate being recessed a distance within an opening of said passivation layer;

forming an opening in said passivation layer at the location of said at least one conductive pad of said at lest one lead of said first substrate;

attaching said first substrate to said second substrate, said at least one conductive pad of said at least one lead of said second substrate extending a distance within an opening of said passivation layer of said first substrate; and

abutting said flat surface area of said at least one conductive pad of said at least one lead of said first substrate against said flat surface area of said at least one conductive pad of said at least one lead of said second substrate; and

forming a direct sliding movable contact between said flat surface area of said at least one conductive pad of said at least one lead of said first substrate and said flat surface area of said at least one conductive pad of said at least one lead of said second substrate, and establishing electrical communication therebetween.

9 10. The method of claim ~~9~~ 6, wherein the step of attaching said first substrate to said second substrate further comprises:

forming a passivation layer by providing said passivation layer on said first surface of said first substrate, and

attaching said passivation layer to said first surface of said second substrate with a layer of adhesive.

10 11. The method of claim ~~9~~ 8, wherein the step of attaching said first substrate to said second substrate further comprises:

forming a passivation layer by providing said passivation layer on said first surface of said second substrate; and attaching said passivation layer to said first surface of said first substrate with a layer of adhesive.

11 ~~12~~. The method of claim ~~9~~ 8, wherein the step of attaching said first substrate to said second substrate further comprises:

covering a portion of one of said first substrate and said second substrate with glob top material which adheres to the first surface of one of said first substrate and said second substrate.

12 ~~13~~. The method of claim ~~9~~ 8, wherein the step of attaching said first substrate to said second substrate further comprises:

encapsulating said first substrate and said second substrate with an encapsulation material.

13 ~~14~~. The method of claim ~~9~~ 8, wherein at least one of said first substrate first surface and said second substrate first surface includes at least one groove thereon.

14 ~~15~~. The method of claim ~~9~~ 8, wherein at least one of said first substrate and said second substrate comprises a flip chip.

15 ~~16~~. The method of claim ~~9~~ 8, wherein at least one of said first substrate and said second substrate comprises a silicon wafer.

16 ~~17~~. (Amended) An assembly method for a semiconductor assembly, comprising:

providing a first silicon substrate having a plurality of leads on a first surface thereof, each lead of said plurality of leads of said first substrate having a conductive pad disposed thereor in substantially a horizontal plane, each conductive pad of said first substrate having a substantially flat surface area and having a thickness;

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providing a second substrate having a plurality of leads on a first surface thereof in a substantially horizontal plane, each lead of said plurality of leads of said second substrate having a conductive pad disposed thereon, each conductive pad of said second substrate having a substantially flat surface area and having a thickness;

providing a passivation layer on said first surface of said first substrate, said passivation layer having a thickness greater than said thickness of each conductive pad of said first substrate, each said conductive pad of said first substrate being recessed a distance within an opening of said passivation layer;

forming an opening in said passivation layer at the each location of said each conductive pad of said first substrate;

attaching said first substrate to said second substrate, each said conductive pad of said second substrate extending a distance within an opening of said passivation layer of said first substrate; and

abutting said flat surface area of said each conductive pad of said first substrate against said flat surface area of one said conductive pad of said second substrate; and

forming a direct sliding movable contact between said flat surface area of said each conductive pad of said first substrate and said flat surface area of one said conductive pad of said second substrate. and establishing electrical communication therebetween.

17 18. The method of claim 16, wherein the step of attaching said first substrate to said second substrate further comprises:

forming a passivation layer by said providing a passivation layer on said first surface of said first substrate; and

attaching said passivation layer to said first surface of said second substrate with an adhesive.

18 19. The method of claim 16, wherein the step of attaching said first substrate to said second substrate further comprises:

forming a passivation layer by said providing a passivation layer on said first surface of said second substrate; and

attaching said passivation layer to said first surface of said first substrate with an adhesive.

19 20. The method of claim 16, wherein the step of attaching said first substrate to said second substrate further comprises:

covering a portion of one of said first substrate and said second substrate with glob top material which adheres to the first surface of one of said first substrate and said second substrate.

20 21. The method of claim 16, wherein the step of attaching said first substrate to said second substrate further comprises:

encapsulating said first substrate and said second substrate with an encapsulation material.

21 22. The method of claim 16, wherein at least one of said first substrate first surface and said second substrate first surface includes at least one groove thereon.

22 23. The method of claim 16, wherein at least one of said first substrate and said second substrate comprises a flip chip.

23 24. The method of claim 16, wherein at least one of said first substrate and said second substrate comprises a silicon wafer.

24 25. (Amended) An assembly method for a semiconductor assembly, comprising:

providing a first silicon wafer substrate having a plurality of leads on a first surface thereof, each lead of said plurality of leads of said first silicon substrate having a conductive pad disposed on a portion thereof in substantially a horizontal plane, each conductive pad of said first silicon substrate having a substantially flat surface area and having a thickness;

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providing a second silicon substrate having a plurality of leads on a first surface thereof in a substantially horizontal plane, each lead of said plurality of leads of said second silicon substrate having a conductive pad disposed thereon, each conductive pad of said second silicon substrate having a substantially flat surface area and having a thickness;

providing a passivation layer on said first surface of said first silicon substrate, said passivation layer having a thickness greater than said thickness of each said conductive pad of said first silicon substrate, each said conductive pad of said first silicon substrate being recessed a distance within an opening of said passivation layer;

forming an opening in said passivation layer for said each conductive pad of said first silicon substrate;

attaching said first silicon substrate to said second silicon substrate, each said conductive pad of said second silicon substrate extending a distance within an opening of said passivation layer of said first silicon substrate; and

abutting said flat surface area of said each conductive pad of said first silicon substrate against said flat surface area of one said conductive pad of said second silicon substrate; and

forming a direct sliding movable contact between said flat surface area of said each conductive pad of said first silicon substrate against said flat surface area of one said conductive pad of said second silicon substrate, and establishing electrical communication therebetween.

25 ~~26~~. The method of claim ~~25~~ 24, wherein the step of attaching said first silicon substrate to said second silicon substrate further comprises:

forming a passivation layer by providing said passivation layer on said first surface of said first silicon substrate; and

attaching said passivation layer to said first surface of said second silicon substrate with an adhesive.

26 ~~27~~. The method of claim ~~25~~ 24, wherein the step of attaching said first silicon substrate to said second silicon substrate further comprises:

forming a passivation layer by providing said passivation layer on said first surface of said second silicon substrate; and

attaching said passivation layer to said first surface of said first silicon substrate with an adhesive.

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27 28. The method of claim 25, wherein the step of attaching said first silicon substrate to said second silicon substrate further comprises:

covering a portion of one of said first silicon substrate and said second silicon substrate with glob top material which adheres to the first surface of one of said first silicon substrate and said second silicon substrate.

28 29. The method of claim 25, wherein the step of attaching said first silicon substrate to said second silicon substrate further comprises:

encapsulating said first silicon substrate and said second silicon substrate with an encapsulation material.

29 30. The method of claim 25, wherein at least one of said first silicon substrate first surface and said second silicon substrate first surface includes at least one groove thereon.

30 31. The method of claim 25, wherein at least one of said first silicon substrate and said second silicon substrate comprises a flip chip.

Claim 32 is cancelled.